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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,022	BULOVIC ET AL.	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,7,8,12-14,16-18,20,21 and 29-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,7,8,12-14,16-18,20,21 and 29-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 October 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/1/07
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, August 1st, 2007, the Applicant cancelled claims 22, 26-28 and added new claims 29-42. Currently claims 1, 7-8, 12-14, 16-18, 20-21 and 29-42 are pending.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the single embodiment comprising edge *and* top surface photodetectors must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 7-8, 12-14, 16-18, 20-22, and 26-27 have been considered and are not persuasive.

On pages 7-8 of the Remarks, the Applicants argue persuasively that the limitations of claims 7, 16, 18 and 26 are supported by the specification. As such the 112 rejection to these claims has been withdrawn. Applicants are pointed to the above requirement of a drawing showing such an embodiment, however.

On pages 9-10 of the Remarks, the Applicants argue that the combination of Tamura with Yuyama is not sufficient to obviate the claimed limitations of claims 1 and 14. Specifically the Applicants argue that Yuyama does not disclose a transparent substrate having an upper surface proximal to the light emitting device, a lower surface distal from the light emitting devices and a plurality of side surfaces.

The Examiner respectfully disagrees. First it must be noted that Yuyama is not required to disclose a transparent substrate having the claimed surfaces. Tamura sufficiently discloses the transparent substrate limitations. Regardless, Yuyama does disclose a transparent substrate (4 in fig. 11) having an upper surface (south surface of 4 in fig. 11) proximal to light emitting devices (2a-c in fig. 11), a lower surface (north surface of 4 in fig. 11) distal from the light emitting devices and a plurality of side surfaces (west and east edges of 4 in fig. 11). It is quite clear that the south surface of the substrate is proximal to the elements, when the north surface is taken into account.

The Applicants seem to argue that the light elements are not located proximally to the substrate. The Examiner must disagree. The adjectives, proximal and distal, are used to define the two surfaces of the substrate. Therefore it should be clear from figure 11 of Yuyama that the south surface of the substrate is proximal to the light emitting elements when compared to the north surface of the substrate.

It is important to point out the only limitation which Tamura is locating the photodetector on the side opposite of the light emitting devices. Yuyama clearly teaches just that in figure 11. As such when this teaching is combined with Tamura, all of the limitations of claims 1 and 14 will have been met.

As shown above the rejections of claims 1, 7-8, 12-14, 16-18 and 20-22 are seen as sufficient and are thus maintained.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Henmi et al. (US 7,154,492).

With respect to claim 33, Henmi discloses an array (fig. 12; for example), comprising a plurality of light emitting devices (20 in fig. 4) disposed over a substrate

(11 in fig. 4), and a photodetector (23 in fig. 4) that detects light emitted through the substrate from the light emitting device (clear from fig. 4), wherein at least one light emitting device comprises an OLED (col. 1, line 9).

With respect to claim 34, Henmi discloses, the array of claim 33 (see above), further comprising a feedback circuit (40-43 in fig. 5) that measures a brightness level for each of the plurality of light emitting devices, and varies a voltage applied to individual ones of the light emitting devices to maintain a brightness level of each of the light emitting devices at a substantially constant level (clear from fig. 9).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 7-8, 13-14, 16-17, 20, 22 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 2002/0130326) in view of Yuyama et al. (US 6,069,676).

With respect to claim 1, Tamura discloses, an array, comprising:

a plurality of light emitting devices (12-14 in fig. 3a,b) disposed over a transparent substrate (10 in fig. 3b), the transparent substrate having an upper surface (bottom of 10 in fig. 3b) proximal to the light emitting devices, a lower surface distal from the light emitting devices (top of 10 in fig. 3b) and a plurality of side surfaces (right side

of 10 in fig. 3b), each of the side surfaces being substantially perpendicular to the upper surface (clear from fig. 3b); and

at least one photodetector (15-17 in fig. 3a/b) that detects light emitted through the substrate from the light emitting devices (para. 45).

Tamura does not expressly disclose that the at least one photodetector is arranged on the lower surface of the transparent substrate.

Yuyama discloses, an array, comprising:

a plurality of light emitting devices (2a-c in fig. 11) disposed under a transparent substrate (4 in fig. 11); and

at least one photodetector (10 in fig. 11) arranged on an opposite surface of the transparent substrate (clear from fig. 11) for detecting light emitted through the substrate from the light emitting devices.

Yuyama and Tamura are analogous art because they are both from the same field of endeavor namely, detecting light emitted by LEDs and compensating the driving of the LEDs based on the detected light.

At the time of the invention it would have been obvious to one or ordinary skill in the art to locate the photosensors of Tamura on the lower surface (top of 10 in fig. 3b) of the transparent substrate of Tamura, as taught by Yuyama.

The motivation for doing so would have been to avoid obstructing the exiting light (Yuyama; col. 6, lines 32-35).

With respect to claim 7, Tamura and Yuyama disclose, the array of claim 1 (see above).

The above embodiment of Tamura fails to disclose locating a photodetector over outer periphery edges of the upper surface.

Tamura further discloses in an alternative embodiment, locating a photodetector (9 in fig. 2a/b) over outer periphery edges of the upper surface (10 in fig. 2b).

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine the alternative embodiment of Tamura teaching of upper surface photodetectors with the already combined first embodiment of Tamura and Yuyama, which teaches lower surface photodetectors.

The motivation for doing so would have been to achieve a more accurate feedback detection signal.

With respect to claim 8, Tamura and Yuyama disclose, the array of claim 1 (see above).

Tamura further discloses, a feedback circuit (5 in fig. 1) that measures a brightness level for each of the plurality of light emitting devices and varies a voltage applied to individual ones of the light emitting devise to maintain a brightness level of each of the light emitting devices at a substantially constant level (paras. 12-13).

It should be noted that Yuyama additionally discloses, a feedback circuit (11a-c in fig. 5) that measures a brightness level for each of the plurality of light emitting devices and varies a voltage applied to individual ones of the light emitting devise to maintain a brightness level of each of the light emitting devices at a substantially constant level (col. 3, lines 46-54; for example).

With respect to claim 13, Tamura and Yuyama disclose, the array of claim 1 (see above).

Tamura further discloses, a display (col. 1, lines 6-8) comprising an array of light emitting devices.

With respect to claim 14, Tamura discloses, a method for forming an array, comprising:

forming a plurality of light emitting devices (12-14 in fig. 3a/b) disposed over a transparent substrate (10 in fig. 3b), said transparent substrate having an upper surface (bottom of 10 in fig. 3b) proximal to the light emitting devices, a lower surface distal from the light emitting devices (top of 10 in fig. 3b) and at least one side surface (right side of 10 in fig. 3b) substantially perpendicular to said upper surface of the substrate; and

forming a photodetector (15-17 in fig. 3a/b) that detects light emitted through the substrate from the light emitting devices (para. 45).

Tamura does not expressly disclose that the at least one photodetector is arranged on the lower surface of the transparent substrate.

Yuyama discloses, a method for forming an array, comprising:

forming a plurality of light emitting devices (2a-c in fig. 11) disposed under a transparent substrate (4 in fig. 11); and

forming at least one photodetector (10 in fig. 11) arranged on an opposite surface of the transparent substrate (clear from fig. 11) for detecting light emitted through the substrate from the light emitting devices.

At the time of the invention it would have been obvious to one or ordinary skill in the art to locate the photosensors of Tamura on the lower surface (top of 10 in fig. 3b) of the transparent substrate of Tamura, as taught by Yuyama.

The motivation for doing so would have been to avoid obstructing the exiting light (Yuyama; col. 6, lines 32-35).

With respect to claim 16, Tamura and Yuyama disclose, the method of claim 14 (see above).

Tamura further discloses, forming the photodetector on the side surface of the substrate (clear from fig. 3b).

With respect to claim 17, Tamura and Yuyama disclose, the method of claim 14 (see above).

Tamura further discloses, wherein the photodetector includes a plurality of photodetectors (clear from fig. 3a).

It should be additionally noted that Yuyama also discloses, a plurality of photodetectors (fig. 8; for example).

With respect to claim 20, claim 20 is seen as sufficiently equivalent to claim 8. As such claim 20 is rejected on the same merits shown above in claim 8.

With respect to claim 22, Tamura discloses, a method for maintaining a substantially constant brightness in a plurality of light emitting devices (12-14 in fig. 3a/b) disposed over an upper surface of a transparent substrate (10 in fig. 3b) in an array, comprising:

measuring light emitted from each of the light emitting devices (12-14 in fig. 3a/b; para. 12) by a photodetector (15-17 in fig. 3a/b); and

varying the voltage level applied to each of the light emitting devices to maintain a substantially constant brightness level of light emitted from the light emitting devices (col. 2, lines 26-28; para. 40).

Tamura does not expressly disclose that the photodetector is arranged on the lower surface of the transparent substrate.

Yuyama discloses, a method for maintaining a substantially constant brightness in a plurality of light emitting devices, comprising:

measuring light emitted from each of the light emitting devices (2a-c in fig. 11) by a photodetector (10 in fig. 11) formed on a lower surface of a transparent substrate (4 in fig. 11),

varying the voltage level applied to each light emitting device to maintain a constant brightness level (col. 3, lines 46-54; for example).

At the time of the invention it would have been obvious to one or ordinary skill in the art to locate the photosensors of Tamura on the lower surface (top of 10 in fig. 3b) of the transparent substrate of Tamura, as taught by Yuyama.

The motivation for doing so would have been to avoid obstructing the exiting light (Yuyama; col. 6, lines 32-35).

With respect to claim 26, Tamura discloses, the method of claim 22 (see above).

The above embodiment of Tamura fails to disclose locating a photodetector over outer periphery edges of the upper surface.

Tamura further discloses in an alternative embodiment, locating a photodetector (9 in fig. 2a/b) over outer periphery edges of the upper surface (10 in fig. 2b).

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine the alternative embodiment of Tamura teaching of upper surface photodetectors with the already combined first embodiment of Tamura and Yuyama, which teaches lower surface photodetectors.

The motivation for doing so would have been to achieve a more accurate feedback detection signal.

With respect to claim 27, Tamura and Yuyama disclose, the method of claim 22 (see above).

Tamura further discloses, wherein varying the voltage level applied to each of the light emitting devices further comprises generating a compensation factor for each of the light emitting devices (para. 40) and applying the compensation factor to a voltage applied to the corresponding light emitting device (para. 40).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 2002/0130326) in view of Yuyama et al. (US 6,069,676) and further in view of Cok (US 7,026,597).

With respect to claim 18, Tamura and Yuyama discloses, the method of claim 17 (see above).

Tamura further discloses, that photodetectors are formed on the side surfaces (18 in fig. 3b).

Neither Yuyama nor Tamura expressly disclose, that the photo detectors are formed on each side surface.

Cok discloses, forming photodetectors on each edge of a display (20 in fig. 5).

Cok, Yuyama and Tamura are analogous art because they are from the same field of endeavor namely, placement of photodetectors within a display.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include photodetectors along each side as taught by Cok in the display of Yuyama and Tamura.

The motivation for doing so would have been improved illumination detection (Cok; col. 1, lines 65-67).

10. Claims 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 2002/0130326) in view of Yuyama et al. (US 6,069,676) and further in view of Yamazaki et al. (US 6,424,326).

With respect to claim 12, Tamura and Yuyama disclose, the array of claim 8 (see above).

Tamura further discloses, wherein the feedback circuit (5 in fig. 1) includes a compensation factor generator (5 in fig. 1) for generating a compensation factor for each of the plurality of light emitting devices (para. 40).

Neither Yuyama nor Tamura expressly disclose, a memory array for storing the compensation factor for each of the plurality of light emitting devices.

Yamazaki discloses, a display detecting brightness (fig. 1) and a memory array (204 in fig. 6) for storing a compensation factor for each of the plurality of light emitting devices (col. 12, lines 21-55).

Yamazaki, Yuyama and Tamura are analogous art because they are all directed to a similar problem solving area, namely correcting uneven display luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to store the correction factors generated by Yuyama and Tamura in a memory array as taught by Yamazaki.

The motivation for doing so would have been to store an ideal luminance to compare the current state of the display against, thus achieving a more uniform and ideal luminance (Yamazaki; col. 12, lines 28-44).

With respect to claim 21, as shown above Tamura and Yuyama disclose claim 14. The further limitations of claim 21 are identical to those of claim 12. Therefore claim 21 is rejected on the same merits shown above in claim 12.

11. Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Yuyama et al. (US 6,069,676).

With respect to claim 29, Henmi discloses, an array (fig. 12, for example), comprising:

a plurality of light emitting devices (20 in fig. 3-4) formed (clear from fig. 3) on a surface of a transparent substrate (11 in fig. 3-4); and

at least one photodetector (23 in fig. 4) arranged on a surface of the transparent substrate for detecting light emitted from the light emitting devices (clear from fig. 4).

Henmi does not expressly disclose, wherein the photodetector is arranged on an opposite surface of the transparent substrate.

Yuyama discloses, an array, comprising:

a plurality of light emitting devices (2a-c in fig. 11) disposed under a transparent substrate (4 in fig. 11); and

at least one photodetector (10 in fig. 11) arranged on an opposite surface of the transparent substrate (clear from fig. 11) for detecting light emitted through the substrate from the light emitting devices.

Yuyama and Tamura are analogous art because they are both from the same field of endeavor namely, detecting light emitted by LEDs and compensating the driving of the LEDs based on the detected light.

At the time of the invention it would have been obvious to one or ordinary skill in the art to locate one of the photosensors of Henmi on the opposite surface (top of 10 in fig. 4) of the transparent substrate of Henmi, as taught by Yuyama.

The motivation for doing so would have been to avoid obstructing the exiting light (Yuyama; col. 6, lines 32-35).

With respect to claim 30, Henmi and Yuyami disclose, the array of claim 29 (see above).

Henmi further discloses, at least one additional photodetector (23b in fig. 11) formed over the outer periphery edges of the surface of the transparent substrate (clear from fig. 4).

With respect to claim 31, Henmi and Yuyami disclose, the array of claim 29 (see above).

Henmi further discloses, a feedback circuit (40-43 in fig. 5) that measures a brightness level for each of the plurality of light emitting devices, and varies a voltage applied to individual ones of the light emitting devices to maintain a brightness level of each of the light emitting devices at a substantially constant level (clear from fig. 9).

12. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Yuyama et al. (US 6,069,676) and further in view of Yamazaki et al. (US 6,424,326).

With respect to claim 32, Henmi and Yuyami disclose, the array of claim 31 (see above).

Henmi further discloses, wherein the feedback circuit includes a compensation factor generator (s15 in fig. 9) for generating a compensation factor for each of the plurality of light emitting devices (s16-s17 in fig. 9).

Neither Henmi nor Yuyami expressly disclose, a memory array for storing the compensation factor for each of the plurality of light-emitting devices.

Yamazaki discloses, a display detecting brightness (fig. 1) and a memory array (204 in fig. 6) for storing a compensation factor for each of the plurality of light emitting devices (col. 12, lines 21-55).

Yamazaki, Yuyama and Henmi are analogous art because they are all directed to a similar problem solving area, namely correcting uneven display luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to store the correction factors generated by Yuyama and Henmi in a memory array as taught by Yamazaki.

The motivation for doing so would have been to store an ideal luminance to compare the current state of the display against, thus achieving a more uniform and ideal luminance (Yamazaki; col. 12, lines 28-44).

13. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Yamazaki et al. (US 6,424,326).

With respect to claim 35, Henmi discloses, the array of claim 34 (see above), wherein the feedback circuit includes a compensation factor generator (s15 in fig. 9) for generating a compensation factor for each of the plurality of light emitting devices (s16-s17 in fig. 9).

Henmi does not expressly disclose, a memory array for storing the compensation factor for each of the plurality of light-emitting devices.

Yamazaki discloses, a display detecting brightness (fig. 1) and a memory array (204 in fig. 6) for storing a compensation factor for each of the plurality of light emitting devices (col. 12, lines 21-55).

Yamazaki and Henmi are analogous art because they are all directed to a similar problem solving area, namely correcting uneven display luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to store the correction factors generated by Henmi in a memory array as taught by Yamazaki.

The motivation for doing so would have been to store an ideal luminance to compare the current state of the display against, thus achieving a more uniform and ideal luminance (Yamazaki; col. 12, lines 28-44).

14. Claims 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Hunter (US 6,356,029).

With respect to claim 36, Henmi discloses an array (fig. 12; for example), comprising a plurality of light emitting devices (20 in fig. 4) disposed over a substrate (11 in fig. 4), and a photodetector (23 in fig. 4) that detects light emitted through the substrate from the light emitting device (clear from fig. 4), wherein at least one light emitting device comprises an OLED (col. 1, line 9).

Henmi does not expressly disclose a PLED.

Hunter discloses a PLED display suffering from ageing effects (col. 2, lines 31-37).

Hunter and Henmi are analogous art because they are both directed to solving the same problem namely, degradation of display quality over time in EL devices.

At the time of the invention it would have been obvious to replace the OLED devices of Henmi with the PLED elements of Hunter.

The motivation for doing so would have been the ease of fabrication of PLED elements (Hunter; col. 1, lines 23-26).

With respect to claim 37, Henmi and Hunter disclose, the array of claim 36 (see above).

Henmi further discloses, a feedback circuit (40-43 in fig. 5) that measures a brightness level for each of the plurality of light emitting devices, and varies a voltage applied to individual ones of the light emitting devices to maintain a brightness level of each of the light emitting devices at a substantially constant level (clear from fig. 9).

15. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Hunter (US 6,356,029) and further in view of Yamazaki et al. (US 6,424,326).

With respect to claim 38, Henmi and Hunter disclose, the array of claim 37 (see above).

Henmi further discloses, wherein the feedback circuit includes a compensation factor generator (s15 in fig. 9) for generating a compensation factor for each of the plurality of light emitting devices (s16-s17 in fig. 9).

Neither Hunter nor Henmi expressly disclose, a memory array for storing the compensation factor for each of the plurality of light-emitting devices.

Yamazaki discloses, a display detecting brightness (fig. 1) and a memory array (204 in fig. 6) for storing a compensation factor for each of the plurality of light emitting devices (col. 12, lines 21-55).

Yamazaki, Hunter and Henmi are analogous art because they are all directed to a similar problem solving area, namely correcting uneven display luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to store the correction factors generated by Hunter and Henmi in a memory array as taught by Yamazaki.

The motivation for doing so would have been to store an ideal luminance to compare the current state of the display against, thus achieving a more uniform and ideal luminance (Yamazaki; col. 12, lines 28-44).

16. Claims 39-40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Bawendi et al. (US 6,501,091).

With respect to claim 39, Henmi discloses an array (fig. 12; for example), comprising a plurality of light emitting devices (20 in fig. 4) disposed over a substrate (11 in fig. 4), and a photodetector (23 in fig. 4) that detects light emitted through the substrate from the light emitting device (clear from fig. 4), wherein at least one light emitting device comprises an OLED (col. 1, line 9).

Henmi does not expressly disclose a QDLED.

Bawendi discloses a QDLED display (title).

Bawendi and Henmi are analogous art because they are both from the same field of endeavor namely, high quality LED based displays.

At the time of the invention it would have been obvious to replace the OLED devices of Henmi with the QDLED elements of Bawendi.

The motivation for doing so would have been the availability of additional color choices (Bawendi; col. 1, lines 35-53).

With respect to claim 40, Henmi and Bawendi disclose, the array of claim 39 (see above).

Henmi further discloses, a feedback circuit (40-43 in fig. 5) that measures a brightness level for each of the plurality of light emitting devices, and varies a voltage

applied to individual ones of the light emitting devices to maintain a brightness level of each of the light emitting devices at a substantially constant level (clear from fig. 9).

With respect to claim 42, Henmi, when combined with Bawendi, discloses a display (Henmi; col. 1, line 7) comprising the array of claim 39 (see above).

17. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henmi et al. (US 7,154,492) in view of Bawendi et al. (US 6,501,091) and further in view of Yamazaki et al. (US 6,424,326).

With respect to claim 41, Henmi and Bawendi disclose, the array of claim 40 (see above).

Henmi further discloses, wherein the feedback circuit includes a compensation factor generator (s15 in fig. 9) for generating a compensation factor for each of the plurality of light emitting devices (s16-s17 in fig. 9).

Neither Bawendi nor Henmi expressly disclose, a memory array for storing the compensation factor for each of the plurality of light-emitting devices.

Yamazaki discloses, a display detecting brightness (fig. 1) and a memory array (204 in fig. 6) for storing a compensation factor for each of the plurality of light emitting devices (col. 12, lines 21-55).

Yamazaki, Bawendi and Henmi are analogous art because they are all directed to a similar problem solving area, namely correcting uneven display luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to store the correction factors generated by Bawendi and Henmi in a memory array as taught by Yamazaki.

The motivation for doing so would have been to store an ideal luminance to compare the current state of the display against, thus achieving a more uniform and ideal luminance (Yamazaki; col. 12, lines 28-44).

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
10/3/07

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER